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application, form which the half value width is derived, depends on process parameters including "unit time." To help the Examiner understand the meaning of the unit time in this art, applicant submits with this response a technical paper entitled "Numerically Controlled Dry Etching Technology for Flattening of Si Wafer which Employs SF_6/H_2 Downstream Plasma," of which applicant himself is one of the coauthors. As shown in FIG. 4 of this paper, persons skilled in this art would understand that the unit time for generating an etching rate distribution peak is one minute. Accordingly, persons skilled in the art would choose a material for etching, decide etching conditions, etch the material for one minute, and measure the half value width of the etching rate distribution peak thus obtained. The obtained half value width is a definite length and thus can be compared to any other length.

Claims 2, 3, 8 and 9 have been rejected under 35 USC 112, second paragraph, as indefinite. Applicant respectfully traverses this rejection.

In this Action the Examiner does not repeat his argument in the previous Action that the variation of the wafer size relative to the wafer table size makes the claims indefinite and relies solely on the argument that the half value width is not a definite length to which the wafer size or the wafer table size can be compared, focusing on the meaning of the unit time. Paragraph 3 and Response to Amendment of the Action.

Applicant respectfully disagrees. As explained above, based on the language of the claims and related description in the specification, persons skilled in the art would first choose a wafer for etching, determine etching conditions of the wafer material including a nozzle size and gas species in plasma, etch the wafer using the determined etching conditions for one minute, obtain an etching rate distribution peak of the wafer, measure the half value width of the obtained etching rate distribution peak and use the half value width and the wafer size to determine the wafer table size of the claimed etching apparatus.

In the Response to Amendment section of the Action, the Examiner quotes the guideline from the MPEP which states, "When a term of degree is present, [the Examiner should] determine whether a standard is disclosed or whether one of ordinary skill in the art would be apprised of the scope of the claim." As explained above, persons of ordinary skill in the art would clearly understand the scope of the claims based on the claim language, the disclosure in the specification and the evidence of the level of knowledge of persons skilled in the art represented by the attached article. Thus, this rejection should be withdrawn.

Claims 2, 3, 8 and 9 have been rejected under 35 USC 103(a) as unpatentable over U.S. Patent No. 5,980,769 (Yanagisawa) in view of U.S. Patent No. 6,136,213 (Shinozuka). Applicant respectfully traverses this rejection.

In the previous amendment, applicant explained that neither Yanagisawa nor Shinozuka teaches or suggests that the difference between the radius of the semiconductor wafer and the radius of the wafer table is 10 to 40 percent of the half value width of the etching rate distribution peak. In the Response to Amendment section of the pending Action, the Examiner does not respond to this argument. Instead, in paragraph 5 of this Action the Examiner basically repeats the same argument as in the previous Action. In short, the Examiner finds that Yanagisawa teaches a 7 mm nozzle size and a 30 mm nozzle size for the etching, and Shinozuka provides an etching rate distribution peak similar to that shown in FIG. 2 of this application. Based on this, the Examiner alleges, the difference in radius between the wafer and the wafer table is 3.5 to 15 mm because the center of the nozzle must reach the edge of the wafer and when the nozzle is located at such a position the reactive gas flux not hitting the wafer surface must hit the wafer table surface. Relying on this finding, the Examiner alleges that the size limitation of claim 3, i.e., the radius size difference of 4 to 10 mm, is taught by the combination of the two cited references. The Examiner further seems to argue that because the radius size limitation of claim 3 is allegedly taught by the combination of the references, claim 2, the parent claim of claim 3, must be taught by the same references as well because it is broader than claim 3.

Applicant respectfully submits that the Examiner's logic does not withstand scrutiny. To reject claim 3 as obvious, the Examiner must find in the combined references evidence of the claimed relationships of the radial size of the wafer and wafer table relative to the half value width and the numerical size difference between the wafer and the wafer table. All the Examiner finds in the art, even under his view of it, is the numerical limitation of claim 3. Even if an etching apparatus includes a wafer and a wafer table meeting the numerical limitation added by claim 3, it does not follow that such an apparatus meets the limitation of claim 2, which is incorporated by reference into claim 3, that the difference between the radii of the wafer and the wafer table is 10 to 40 percent of the half value width. The half value width depends significantly on etching conditions including the material for etching and plasma gas species. Simply arriving at the numerical limitation added by claim 3 does not assure that a person of ordinary skill in the art will arrive at the etching apparatus of claim 2 or any claim depending therefrom. Thus, this rejection fails.

In addition, in finding a teaching in the prior art of the numerical limitation of claim 3 the Examiner incorrectly assumed that when the nozzle is located at the edge of the wafer the reactive gas flux not hitting the wafer surface must hit the wafer table surface. Neither Yanagisawa nor Shinozuka provides support for such an assumption, nor does the Examiner point to any other evidence in the prior art that would support such an assumption.

The Examiner provides the same argument in support of rejecting claim 8, which includes the same size limitation relative to the half value width as claim 2. Thus, the rejection of claims 2, 3, 8 and 9 over Yanagisawa and Shinozuka should be withdrawn.

In light of the above, a Notice of Allowance is solicited.

In the event that the transmittal letter is separated from this document and the Patent and Trademark Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to

Deposit Account No. 03-1952, referencing Docket No. 506212000600.

Respectfully submitted,

Dated: May 11, 2004

By: _____

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Numerically Controlled Dry Etching Technology for Flattening of Si Wafer which Employs SF_6/H_2 Downstream Plasma

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Technology for the damage-free flattening of a Si wafer that employs a numerically controlled local dry etching (NC-LDE) technology has been developed to meet the requirement for achieving an extremely flat-surface wafer for the downscaling of ULSI feature size. In this technology, fluorine atoms which are generated in a localized SF_6/H_2 downstream plasma are exposed at a local area of a Si wafer, thereby generating a high etch rate of 130 μm/min at the bottom of the etched profile and a volume removal rate of 45.9 mm^3/min. The flattening process was carried out by numerically controlled scan etching according to previously measured thickness data and consequently site flatness was improved from 0.51 μm to 0.08 μm within 150 s for a 200-mm-diameter Si wafer. This level of flatness will be the value required after 2005. Damage-free characteristics were also confirmed by minority carrier recombination lifetime and sub-surface defect measurements.
[DOI: 10.1143/JJAP.41.2791]

KEYWORDS: NC-LDE, fluorine atoms, SF_6, Si wafer, flattening, numerical control, local etching

1. Introduction

As the minimal feature size of ULSI devices is downscaled to submicron size, an extremely flat surface is required for a Si wafer to enhance resolution in lithography, because resolution and depth of focus (*DOF*) depend on λ/NA and λ/NA^2, respectively, where λ and *NA* are the wavelength of a light source and the numerical aperture, respectively. Therefore, an increase in *NA* results in a narrower *DOF*. The International Technology Roadmap for Semiconductors (ITRS)[1] predicts that site flatness of 130 nm and 100 nm for the Si wafer will be required by 2002 and 2005, respectively.

The conventionally used lapping or polishing technology which employs slurries and pads is considered difficult to use and control to maintain site flatness[2] at a high yield for a 200-mm-diameter Si wafer. In order to resolve this issue, plasma-assisted chemical etching (PACE) technology was developed by Mumola *et al.* in 1991.[3] In PACE, the unevenness distribution in a wafer surface is measured before the flattening process, and then the Si wafer surface is flattened by the numerically controlled etching of locally thick portions with an RF plasma confined to 50 mm diameter. This technology has attracted considerable attention, since it has achieved a high level of flatness that could not be obtained using conventional polishing technologies. However, PACE technology exposes the plasma directly on the Si surface, thereby leading to drawbacks such as ion-induced damage, fluorine atom invasion and sulfur deposition. These have caused slight roughness on the wafer surface called "haze" which was detected as a long-wavelength component of localized light scatters (LLS). In addition, since the Si wafer was used as an anode for RF discharge, Si etch rates in the wafer distributed corresponding to the variation of resistivity within the wafer and the conductivity type of the wafer. Therefore, a software program for compensating resistivity across the entire wafer surface was necessary to flatten the wafer precisely. PACE technology, which depends strongly on wafer characteristics and intricate operation, was not easy to introduce to the mass-production line as the final flattening process of Si wafers.

We have developed a new damage-free flattening technology for a Si wafer, which employs numerically controlled local SF_6/H_2 downstream plasma based on chemical dry etching (CDE)[4] technology to overcome this difficult issue in future wafer flattening technology. The numerically controlled local dry etching, called NC-LDE, is expected to realize damage-free flattening because of the use of only neutral fluorine atoms for Si etching. In addition, this technology shows possibility for application in other processes such as ultra flattening of a leticle mask made of quartz. In this paper, we report the principle of the NC-LDE technology which uses a local SF_6/H_2 downstream plasma and its flattening performance for a Si wafer.

2. Experiment

The experimental apparatus is shown in Fig. 1. A 200-mm-diameter Si wafer was transferred from a load-locked chamber to a process reactor chamber via an alignment chamber. The alignment process is necessary to match the coordinate systems of the wafer thickness measurement apparatus and the flattening process. To etch locally across the entire wafer surface, the wafer that was held on a stage by electostatic chucking was scanned in the *X*–*Y* direction

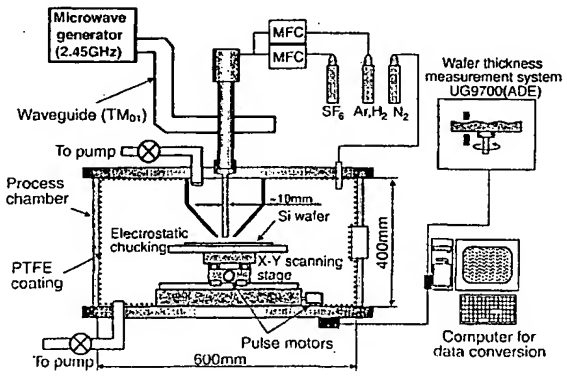

Fig. 1. Schematic diagram of the NC-LDE apparatus which uses SF_6/H_2 downstream plasma for Si wafer flattening.

by driving two pulse motors. The process chamber 600 mm in width, 600 mm in length and 400 mm in height, was made of a stainless steel (SUS) and its inner wall surface was coated with polytetrafluoroethylene (PTFE). The PTEF coating was used to prevent particle generation that occurs with fluorination of SUS material. An alumina discharge tube 32 mm in diameter was inserted into an E-surface waveguide of 2.45 GHz microwave and the SF_6, H_2 and Ar gas mixture was introduced into the top of the discharge tube. The bottom of the tube was fixed on the upper plate of the chamber and was connected to a nozzle 10 mm in diameter and 105 mm in length. Fluorine atoms produced by the SF_6 discharge were transported to limited areas of the Si surface by means of the nozzle; the distance between the nozzle and the wafer surface was 10 mm. A differential exhaust tube made of aluminum was fixed coaxially around the nozzle. N_2 gas was introduced into the vacuum chamber to prevent diffusion of F atoms located outside of the differential exhaust tube into the reactor. Therefore, both N_2 gas and F atoms are removed through a gap between the nozzle and the differential exhaust tube edges.

Figure 2 shows the Si wafer flattening process utilizing NC-LDE technology. First, prior to the flattening process, the wafer thickness was measured using a thickness measurement system (ADE Corp., Ultra Gage 9700) and the thickness distribution data were converted to thickness data, $T(x,y)$ in 1-mm-grid format, where x and y are the coordinates of the grid for the wafer. The amount of local etching was represented by an etching profile $P(r)$ which was expressed by the shape etched off below the nozzle as a function of radial distance, r from the nozzle center axis. Then, the thickness data that were converted to the grid format and the etching profile were entered into a computer of the NC-LDE system for data conversion, which determines the optimum scan velocity data, $V(x,y)$, to flatten the wafer. Two pulse motors were driven in accordance with these scan velocity data in order to scan the wafer as seen in the bottom right of Fig. 2. As explained here, the NC-LDE technology allows the shape of the surface to be controlled using the stage scan velocity data. Therefore, not only a flat surface but also three-dimensional shapes such as spherical, non-spherical or cylindrical can be fabricated according to the input shaping data.

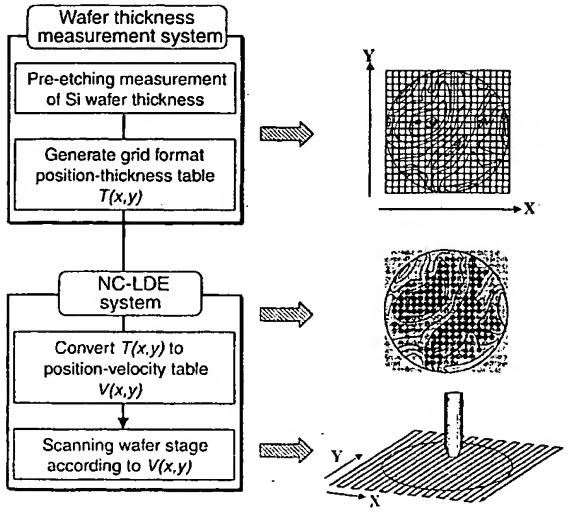

Fig. 2. Flattening process using NC-LDE technology.

3. Result and Discussion

3.1 Characteristics of local dry etching

To etch the Si surface locally, observation of the chemical luminescence[5] that is emitted during Si etching with fluorine atoms is very effective. Figures 3(a) and 3(b) show photographs of the chemical luminescence generated during etching of the Si wafer with and without the N_2 gas introduction to the reactor, respectively. Here the nozzle and differential exhaust tube are made of quartz so that we can observe the inner structure of the differential exhaust system. If N_2 gas is not introduced, one can observe the bright luminescence on the entire Si surface, as shown in Fig. 3(a). This indicates that fluorine atoms of the present etchant diffuse extensively out of the nozzle in spite of the coaxial structure of the differential exhaust tube. On the other hand, the luminous region was limited to the area immediately surrounding of the nozzle when N_2 gas of 1500 sccm was introduced to the reactor chamber.

Figure 4(a) shows the Si etching profile for the wafer located exactly below the nozzle using the 90% SF_6, 9% Ar, and 1% H_2 mixture, where the gas pressure measured at the inlet of the discharge tube, the N_2 introduction to confine the etching region and the microwave power are 106 Pa,

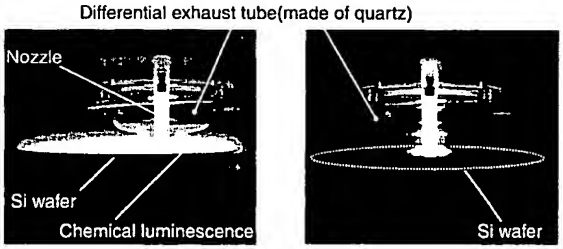

Fig. 3. Etching of 200-mm-diameler Si wafer (a) without N_2 introduction and (b) with N_2 introduction.

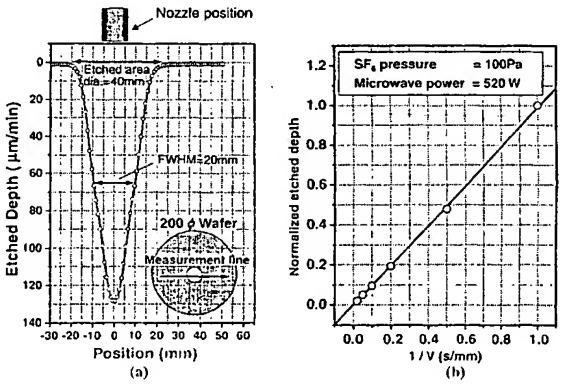

Fig. 4. (a) Etching profile and (b) the relationship between normalized etched depth and inverse of scan velocity.

1500 sccm and 560 W, respectively. Ar gas was added to facilitate the ignition. The reason for the Ar addition is explained as follows; since a number of negative fluorine ions are generated as a result of the process of electron attachment dissociation of SF_6 in the plasma, it is not easy to generate SF_6 alone in plasma. Hence electrons are supplied into SF_6 plasma by means of Ar plasma generation. The 1% H_2 addition plays a role of suppressing of the cloudy texture that appears after etching of Si. In the beginning of this study, the existence of the cloudy texture was a problem. It did not appear on the Si surface when the wafer was fixed under the nozzle. However, a texture consisting of a number of cloudy lines appeared after scanning the wafer as shown in Fig. 5. Fortunately, the 1% addition of H_2 gas caused the cloudy texture to disappear completely. Clarification of the mechanism of this phenomenon based on a study on the surface reaction will be reported elsewhere.

Figure 6 shows the microwave power dependence of Si etch rate with SF_6 flow rate as a parameter. The higher the microwave power and flow rate, the higher the Si etch rate. In particular, the Si etch rate increased rapidly from about 350 W at SF_6 flow rate of 500 sccm in contrast to the slowly increasing etch rate at SF_6 flow rate of 300 sccm. This implies that the dissociation of SF_6 depends strongly on both parameters. To understand the reason why the SF_6 dissociation occurs under higher microwave power and flow rates, the relationship among SF_6 flow rate, Si etch rate and total gas pressure when microwave power is fixed at 500 W was investigated, and the result are shown in Fig. 7. SF_6 pressure increased in proportion with increasing SF_6 flow rate. On the other hand, Si etch rate showed a maximum at approximately 500 sccm and decreased with higher flow rates. The decreased etch rate at higher flow rate is considered to result from the reduced dissociation rate of SF_6 due to the decrease in electron temperature which was lowered by the elevation in pressure. Therefore, microwave power of 500 W and flow rate of 500 sccm were found to be the conditions that achieved the highest etch rate in our present system.

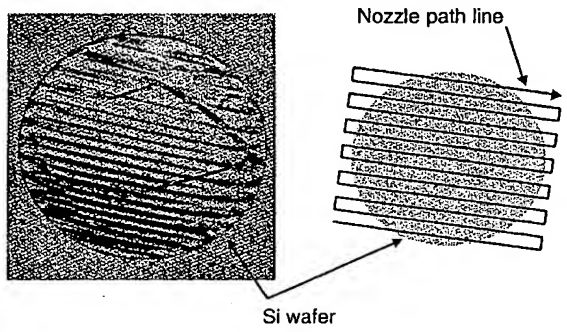

Fig. 5. Cloudy texture generated on Si surface.

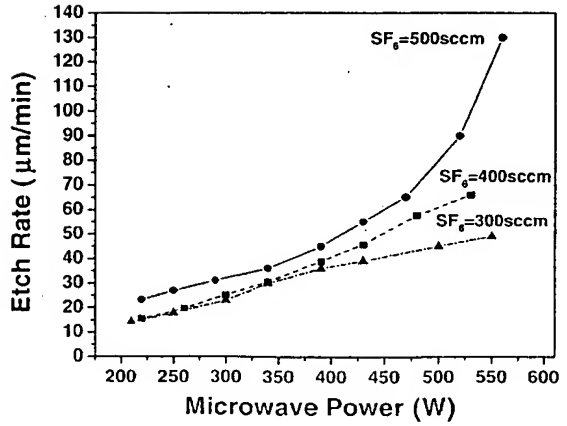

Fig. 6. Microwave power dependence of Si etch rate with SF_6 flow rate as a parameter.

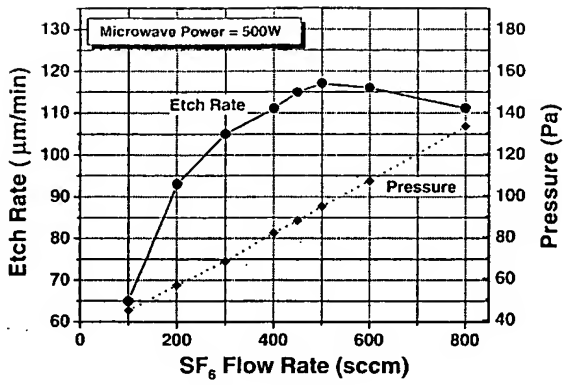

Fig. 7. Relationship among SF_6 flow rate, Si etch rate and total gas pressure. Microwave power is fixed at 500 W.

The etching profile was axially symmetric around the center point of the etching region. The etched area was confined to 40 mm diameter owing to the differential exhaust tube and the N_2 introduction. Here, the etching profile is described as a function of the depths and the distances from the center point of the etching region in older to input the profile into the computer. In this experiment, the local Si etch rate is defined in the following two ways. The peak etch rate (*PER*) which is the etch rate at the deepest point, is 130 μm/min and volume removal rate (*VRR*), which is the removal volume per unit time, was evaluated using the following formula to be 45.9 mm^3/min.

$$VRR = \iint P(r) r \, dr \, d\theta, \tag{1}$$

where the cross section of the etching profile was approximated to the Gaussian function and $P(r)$ is the etching depth profile at a unit time as a function of radius, r from the etching center point. A higher etch rate can lead to shorter processing time which can be achieved by increasing the average scan velocity. However, the higher etch rate causes slight etching of the Si surface even if the scan velocity is very high, thereby reducing the precision of the wafer flattening. Therefore, the optimum etch rate must be determined with consideration of the average scan velocity to obtain the maximum throughput for the flattening process and the minimum etched depth under high scan velocities.

Figure 4(b) shows the relationship between the inverse of scan velocity of the Si wafer for the fixed nozzle and the normalized etched depth. In this experiment, the wafer was moved in a straight line and at a constant velocity below the nozzle. The etched depth is almost completely inversely proportional to scan velocity $V(x, y)$. Hence the etched depth

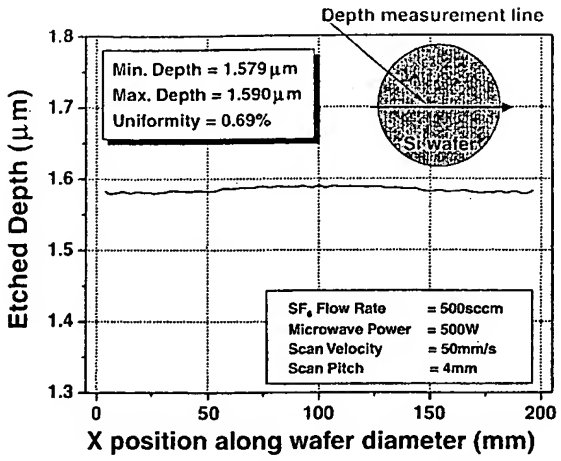

Fig. 8. Variation of Si etched depth along 200-mm-diameter wafer when the local etching is carried out at a constant velocity of 50 mm/s, and a fixed pitch of 4 mm.

can be adjusted precisely by controlling the scan velocity. In the actual flattening process, the effect of the scanning overlapping in the adjacent regions should be considered, when the local etching was scanned at 4 or 5 mm pitch.

Figure 8 shows the variation of Si etched depth along 200-mm-diameter wafer when the local etching is carried out at a constant velocity of 50 mm/s and a fixed pitch of 4 mm. The variation of 0.69% demonstrates excellent uniformity. The etching time was about 4.0 min. This indicates that the etch rate hardly varies with time.

3.2 *Flattening performance of numerically controlled dry etching*

A 200-mm-diameter Si wafer was flattened using NC-LDE technology which employs the SF_6/H_2 downstream plasma, where the plasma was generated using 90% SF_6, 9% Ar, 1% H_2 mixture at a pressure of 110 Pa and a microwave power of 520 W. Local etching was performed using a nozzle 13 mm in diameter and N_2 introduction at 1500 sccm to the reactor. *PER* and *VRR* were 60 μm/min and 20 mm^3/min, respectively. Prior to the flattening process, the Si wafer was cleaned using a diluted 1% HF solution to remove the native oxide layer. The native oxide removal is not always necessary, but a clean Si surface without the native oxide layer is preferable to obtain a smooth surface without haze. In this experiment, the convex-shaped wafer was processed, but a concave-shaped wafer also yields the same results. In Fig. 9, site flatness (SBIR; site back-surface total indicator range) of a 25 mm × 25 mm site (a), and global flatness (GBIR; global back-surface total indicator range) of a 200 mm area (b), are shown for measurements carried out before and after the flattening process. These flatness measurements were obtained using an electro capacitance-type probe (ADE Corp., Ultra Gage 9700) with 1.9 mm ring spacing. The average SBIR of all sites was improved from 0.292 μm to 0.048 μm. Maximum SBIR and GBIR were greatly improved from 0.51 to 0.08 μm and 0.8 to 0.12 μm, respectively. The average scan velocity in this flattening process was 65 mm/s and the processing time was 150 s. This flattening result was extremely good and exceeded the

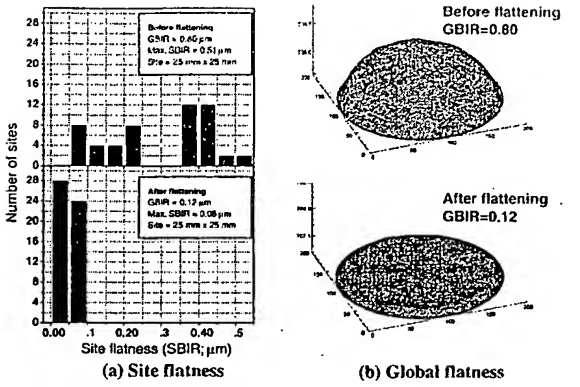

Fig. 9. Flatness change before and after the NC-LDE process. (a) Site flatness distribution and (b) global flatness.

value that is needed in 2008 as predicted by the ITRS.

3.3 *Quality of etched Si surface*

This NC-LDE technology will be used near the final stage of the wafer manufacturing process. Therefore, the integrity of the Si surface without damage and roughness is required for a flattened wafer. Consequently, the etched surface was evaluated for microroughness, carrier recombination lifetime and damage generation. Figures 10(a) and 10(b) show 3D views of 2 μm × 2 μm AFM images of non-etched and etched Si surfaces. Here, half of a mirror- polished 200-mm-diameter Si wafer was etched to a depth of 2 μm and the remaining half was not etched as a reference. In order to etch the Si wafer uniformly to 2 μm depth, the scan stage velocity and the step pitch were 20 mm/s and 5 mm, respectively. The average roughness (R_a) of 0.0745 nm was obtained in the etched area, in contrast to the R_a of 0.0962 nm in the non-etched area. This result suggests that the spatial wavelength of microroughness on the wafer surface does not change after etching. A comparison of the tone texture between these two AFM images reveals that the long-wavelength

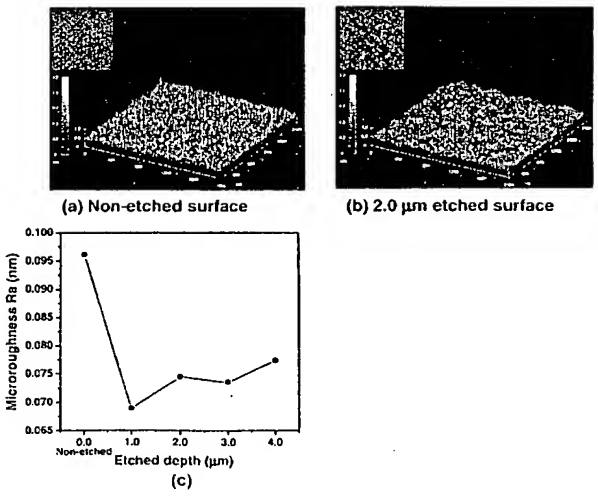

Fig. 10. Microroughnesses of (a) non-etched, and (b) 2 μm etched Si surface and (c) etched depth dependence of microroughness measured by AFM (Olympus, NV2000).

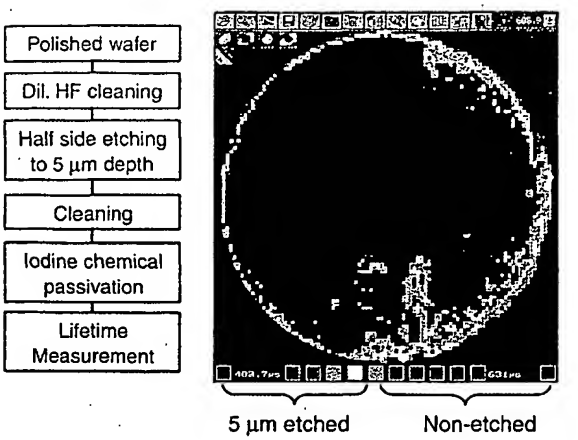

Fig. 11. 2D map of minority carrier recombination lifetime (SEMILAB, WT-85).

component increased in the etched surface. The etched depth dependence of the microroughness is shown in Fig. 10(c). Microroughness was improved after etching and then slightly increased with increasing removal depth. This result indicates that the microroughness of the Si wafer surface does not change before and after this flattening process.

Figure 11 shows a mapping of minority carrier recombination lifetime across the entire surface of an 200-mm-diameter Si wafer using laser-induced and microwave detected photoconductive decay measurement (μ-PCD) method (WT-85 of SEMILAB. Corp). In the same way as the above-mentioned experiment, the left half of the wafer was etched to a depth of 5 μm and the remaining non-etched surface was used as reference in order to clarify the effects of etching. Before the etching process, the wafer was dipped into 1% HF solution for 10 s to remove the native oxide layer and the Si surface after the etching process was passivated chemically by dipping it into a 5.0 wt% iodine in ethanol solution. This iodine chemical passivation process is used to terminate the active Si surface after etching with iodine atoms. No other processes were carried out between the etching and the measurement. Recombination lifetime of the etched surface was longer than that of the non-etched surface. This result indicates that this technology generates no additional damage in the wafer. In addition, even induced damages are removed.

Similar damage evaluation was carried out using another subsurface defect measurement method (VTI Corp., PBS-1000). In this measurement method, a circularly polarized 632.8 nm He–Ne laser was incident to the Si surface at the angle of 55° and a p-polarized component of a back-

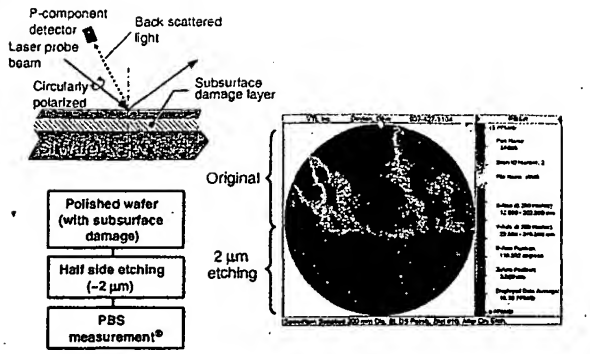

Fig. 12. Subsurface defect map (VTI, PBS-1000).

scattered laser light from the layer with defect was detected. Figure 12 shows the subsurface defect mapping using the backscattering light intensity per unit solid angle. Again, the lower half of a 200-mm-diameter Si wafer was etched to a depth of 2 μm and the remaining upper half was used as a reference. The estimated wafer was one in which damages were induced by the previous chemical mechanical polishing (CMP) process. The backscattered light intensity of the etched area was lower than that of the non-etched area and the damage induced in the polished area was removed in the etched area. This means the sub-surface damage was removed by the etching.

4. Conclusion

The precise and damage-free flattening of the Si wafer using NC-LDE technology which uses SF_6/H_2 downstream plasma has been achieved. By utilizing the high etch rate of 130 μm/min and precise control of etching depth, maximum site flatness (SBIR) and global flatness (GBIR) were improved to 0.08 μm and 0.12 μm with 150 s for a 200-mm-diameter Si wafer, respectively. Microroughness and carrier recombination lifetime were also improved by this technology. Accordingly, the excellent flattening ability and the high surface quality will enable this technology to be applied in the next-generation wafer manufacturing process for 2005.

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